TRANSFER-MOLD TYPE INSULATED TYPE

PS21963-4S



INTEGRATED POWER FUNCTIONS

600V/10A low-loss 5th generation IGBT inverter bridge for three phase DC-to-AC power conversion.

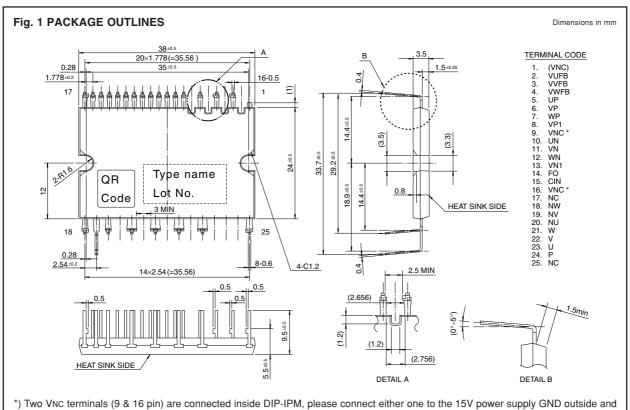
Open emitter type.

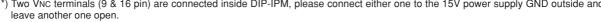
INTEGRATED DRIVE, PROTECTION AND SYSTEM CONTROL FUNCTIONS

- For upper-leg IGBTs: Drive circuit, High voltage high-speed level shifting, Control supply under-voltage (UV) protection.
- For lower-leg IGBTs: Drive circuit, Control supply under-voltage protection (UV), Short circuit protection (SC).
- Fault signaling: Corresponding to an SC fault (Lower-leg IGBT) or a UV fault (Lower-side supply).
- Input interface: 3V, 5V line (High Active).
- UL Approved : Yellow Card No. E80276

APPLICATION

AC100V~200V inverter drive for small power motor control.







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MAXIMUM RATINGS ($T_j = 25^{\circ}C$, unless otherwise noted)

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit
Vcc	Supply voltage	Applied between P-NU, NV, NW	450	V
VCC(surge)	Supply voltage (surge)	Applied between P-NU, NV, NW	500	V
VCES	Collector-emitter voltage		600	V
±IC	Each IGBT collector current	Tc = 25°C	10	Α
±ICP	Each IGBT collector current (peak)	Tc = 25°C, less than 1ms	20	Α
Pc	Collector dissipation	Tc = 25°C, per 1 chip	27.0	W
Tj	Junction temperature	(Note 1)	-20~+125	°C

Note 1: The maximum junction temperature rating of the power chips integrated within the DIP-IPM is 150° C (@ Tc $\leq 100^{\circ}$ C). However, to ensure safe operation of the DIP-IPM, the average junction temperature should be limited to $T_{j(ave)} \leq 125^{\circ}$ C (@ Tc $\leq 100^{\circ}$ C).

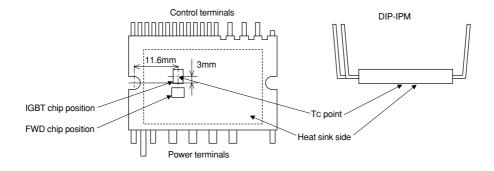
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
VD	Control supply voltage	Applied between VP1-VNC, VN1-VNC 20		V
VDB	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-W 20		V
VIN	Input voltage	Applied between UP, VP, WP, UN, VN, WN-VNC	-0.5~VD+0.5	V
VFO	Fault output supply voltage	Applied between Fo-VNC	-0.5~VD+0.5	V
IFO	Fault output current	Sink current at Fo terminal	1	mA
Vsc	Current sensing input voltage	Applied between CIN-VNC	-0.5~VD+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit
VCC(PROT)	Self protection supply voltage limit (short circuit protection capability)	$VD = 13.5$ ~16.5V, Inverter part $T_j = 125$ °C, non-repetitive, less than 2μs	400	V
Tc	Module case operation temperature	(Note 2)	− 20~+100	°C
Tstg	Storage temperature		− 40~+125	°C
Viso	Isolation voltage	60Hz, Sinusoidal, 1 minute, Between pins and heat-sink plate	1500	Vrms

Note 2: To measurement point





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THERMAL RESISTANCE

0	Davamatav	Condition	Limits			Llmit
Symbol Parameter		Condition		Тур.	Max.	Unit
Rth(j-c)Q	Junction to case thermal	Inverter IGBT part (per 1/6 module)	_	_	3.7	°C/W
Rth(j-c)F	resistance (Note 3)	Inverter FWD part (per 1/6 module)	_	_	4.5	°C/W

Note 3: Grease with good thermal conductivity should be applied evenly with about +100µm~+200µm on the contacting surface of DIP-IPM

and heat-sink. The contacting strate of DIP-IPM case and heat sink (Rth(c-f)) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) (per 1/6 module) is about 0.3° C/W when the grease thickness is $20\mu m$ and the thermal conductivity is $1.0W/m \cdot k$.

ELECTRICAL CHARACTERISTICS (Tj = 25°C, unless otherwise noted)

INVERTER PART

Cumple of	Davamatav	Condition		Limits			Unit	
Symbol	Parameter		Condition		Тур.	Max.	Unit	
VCE(cot)	Collector-emitter saturation	VD = VDB = 15V	Ic = 10A, Tj = 25°C	_	1.70	2.20		
VCE(sat) voltage	VIN = 5V	Ic = 10A, Tj = 125°C	_	1.80	2.30	V		
VEC	FWD forward voltage	$T_j = 25^{\circ}C$, $-IC = 10A$, $VIN = 0V$		_	1.70	2.20	V	
ton		Vcc = 300V, VD = VDB = 15V		0.60	1.10	1.70	μS	
trr				_	0.30	_	μS	
tc(on)	Switching times	IC = 10A, Tj = 125°C, VIN	IC = 10A, Tj = 125°C, VIN = 0 ↔ 5V		0.40	0.60	μS	
toff		Inductive load (upper-lov	Inductive load (upper-lower arm)		1.50	2.10	μS	
tc(off)		, , ,		_	0.50	0.80	μS	
ICES	Collector-emitter cut-off	Vor. Vor.	Tj = 25°C	_	_	1	mA	
lioco	current	VCE = VCES $T_i = 125^{\circ}C$	_	_	10	''''^		

CONTROL (PROTECTION) PART

Cumbal	Parameter	Condition			Limits		Unit	
Symbol	Parameter			Min.	Тур.	Max.		
		VD = VDB = 15V Total of VP1-VNC, VN1-VNC		_	_	2.80		
ID	Circuit current	VIN = 5V	VIN = 5V VUFB-U, VVFB-V, VWFB-W		_	_	0.55	mA
טו	Circuit current	VD = VDB = 15V	Total	of VP1-VNC, VN1-VNC	_	_	2.80	шд
		VIN = 0V	VUFB-	U, VVFB-V, VWFB-W	_	_	0.55	
VFOH	Fault output voltage	Vsc = 0V, Fo terminal pull-up to 5V by $10k\Omega$			4.9	_	_	V
VFOL	Fault output voltage	VSC = 1V, IFO = 1mA			_	_	0.95	V
VSC(ref)	Short circuit trip level	$T_j = 25^{\circ}C, V_D = 15V$ (Note 4)			0.43	0.48	0.53	V
lin	Input current	VIN = 5V		0.70	1.00	1.50	mA	
UVDBt				Trip level	10.0	_	12.0	٧
UVDBr	Control supply under-voltage	T _i ≤ 125°C		Reset level	10.5	_	12.5	V
UVDt	protection	1] 5 125 0		Trip level	10.3	_	12.5	V
UVDr				Reset level	10.8	_	13.0	V
tFO	Fault output pulse width			(Note 5)	20	_	_	μS
Vth(on)	ON threshold voltage				_	2.1	2.6	V
Vth(off)	OFF threshold voltage	Applied between Up Vp Wp Ha Va Wa Vac		0.8	1.3	_	V	
Vth(hys)	ON/OFF threshold hysteresis voltage	Applied between UP, VP, WP, UN, VN, WN-VNC			0.35	0.65	_	٧

Note 4: Short circuit protection is functioning only for the lower-arms. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

5: Fault signal is asserted corresponding to a short circuit or lower side control supply under-voltage failure.



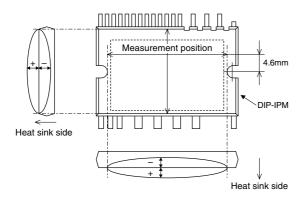
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MECHANICAL CHARACTERISTICS AND RATINGS

Darameter	Condition		Limits			Unit
Parameter	Con	Condition		Тур.	Max.	Offic
Mounting torque	Mounting screw : M3 (Note 6) Recommended : 0.69 N·m		0.59	_	0.78	N·m
Weight		_	10	_	g	
eat-sink flatness (Note 7)		-50	_	100	μm	

Note 6: Plain washers (ISO 7089~7094) are recommended.

Note 7: Flatness measurement position



RECOMMENDED OPERATION CONDITIONS

0	D	Condition		Limits			Llmit
Symbol Parameter		Condition		Min.	Тур.	Max.	Unit
Vcc	Supply voltage	Applied between P-NU, NV, NW		0	300	400	V
VD	Control supply voltage	Applied between VP1-VNC, VN1-VNC		13.5	15.0	16.5	V
VDB	Control supply voltage	Applied between VUFB-U, VVFB-V, VWFB-	W	13.0	15.0	18.5	V
ΔV D, ΔV DB	Control supply variation		-1	_	1	V/μs	
tdead	Arm shoot-through blocking time	For each input signal, Tc ≤ 100°C	1.5	_	_	μS	
fPWM	PWM input frequency	Tc ≤ 100°C, Tj ≤ 125°C			_	20	kHz
lo.	Allowable r.m.s. current	VCC = 300V, VD = VDB = 15V, P.F = 0.8, sinusoidal PWM,	7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7		_	5.0	Arms
lo	Allowable f.m.s. current	$T_j \le 125^{\circ}C$, $T_C \le 100^{\circ}C$ (Note 8)	fPWM = 15kHz	_	_	3.0	Aiiis
PWIN(on)	Allowable minimum input		0.5	_	_	_	
PWIN(off)	pulse width		0.5	_	_	μS	
VNC	VNC variation	Between VNC-NU, NV, NW (including sur	ge)	-5.0	_	5.0	V

Note 8: The allowable r.m.s. current value depends on the actual application conditions.

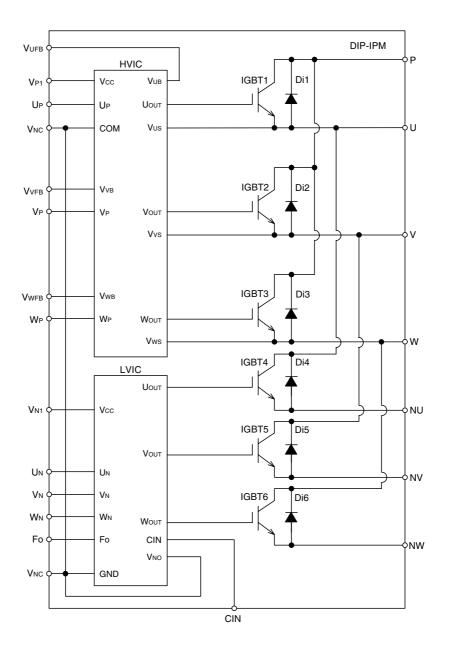


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^{9:} IPM might not make response if the input signal pulse width is less than the recommended minimum value.

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Fig. 2 THE DIP-IPM INTERNAL CIRCUIT



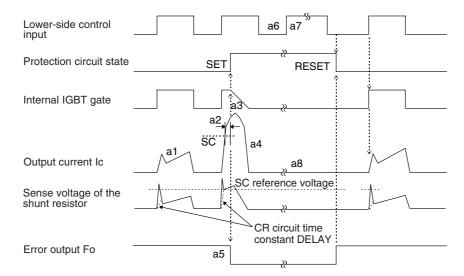


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Fig. 3 TIMING CHART OF THE DIP-IPM PROTECTIVE FUNCTIONS

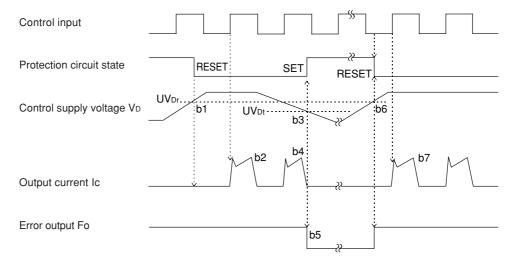
[A] Short-Circuit Protection (Lower-side only with the external shunt resistor and CR filter)

- a1. Normal operation: IGBT ON and carrying current.
- a2. Short circuit detection (SC trigger).
- a3. IGBT gate hard interruption.
- a4. IGBT turns OFF.
- a5. Fo outputs (tFO(min) = 20μ s).
- a6. Input "L": IGBT OFF.
- a7. Input "H": IGBT ON.
- a8. IGBT OFF in spite of input "H".



[B] Under-Voltage Protection (Lower-side, UVD)

- b1. Control supply voltage rising: After the voltage level reaches UVDr, the circuits start to operate when next input is applied. b2. Normal operation: IGBT ON and carrying current.
- b3. Under voltage trip (UVDt).
- b4. IGBT OFF in spite of control input condition.
- b5. Fo outputs (tFO \geq 20 μ s and FO outputs continuously during UV period).
- b6. Under voltage reset (UVDr).
 b7. Normal operation: IGBT ON and carrying current.





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[C] Under-Voltage Protection (Upper-side, UVDB)

- c1. Control supply voltage rising: After the voltage level reaches UVDBr, the circuits start to operate when next input is applied. c2. Normal operation: IGBT ON and carrying current.

- c3. Under voltage trip (UVDBt).
 c4. IGBT OFF in spite of control input signal level, but there is no Fo signal outputs.
- c5. Under voltage reset (UVDBr)
- c6. Normal operation: IGBT ON and carrying current.

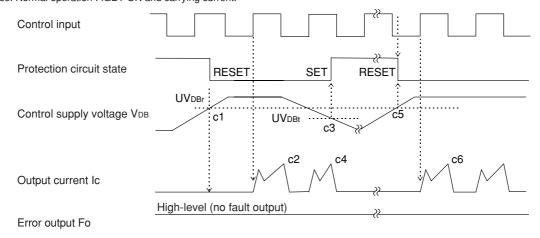
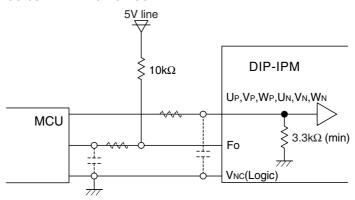


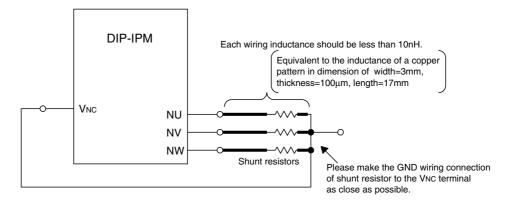
Fig. 4 RECOMMENDED MCU I/O INTERFACE CIRCUIT



Note: The setting of RC coupling at each input (parts shown dotted) depends on the PWM control scheme and the wiring impedance of the printed circuit board.

The DIP-IPM input section integrates a $3.3k\Omega$ (min) pull-down resistor. Therefore, when using an external filtering resistor, pay attention to the turn-on threshold voltage.

Fig. 5 WIRING CONNECTION OF SHUNT RESISTOR

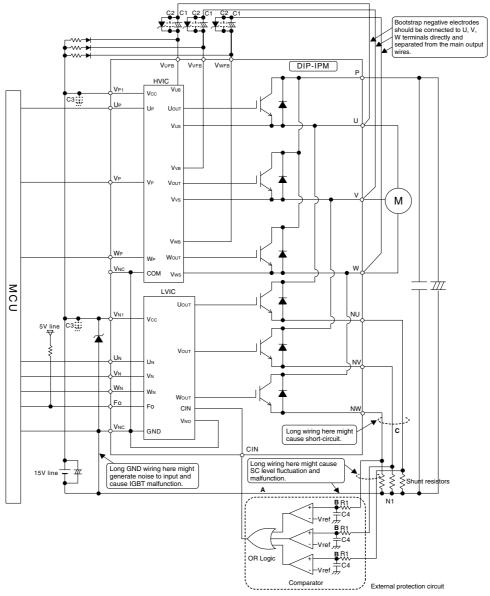




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Fig. 6 AN EXAMPLE OF TYPICAL DIP-IPM APPLICATION CIRCUIT

C1: Electrolytic capacitor with good temperature characteristics C2,C3: 0.22~2µF R-category ceramic capacitor for noise filtering



- Note 1 : Input drive is High-Active type. There is a 3.3kΩ(min.) pull-down resistor integrated in the IC input circuit. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

 Thanks to HVIC inside the module, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

 - 3 : Fo output is open drain type. It should be pulled up to the positive side of a 5V power supply by a resistor of about $10k\Omega$.

 - 4 : To prevent erroneous protection, the wiring of A, B, C should be as short as possible.
 5 : The time constant R1C4 of the protection circuit should be selected in the range of 1.5-2µs. SC interrupting time might vary with the wiring pattern. Tight tolerance, temp-compensated type is recommended for R1, C4.

 6: All capacitors should be mounted as close to the terminals of the DIP-IPM as possible. (C1: good temperature, frequency character-
 - istic electrolytic type, and C2, C3: good temperature, frequency and DC bias characteristic ceramic type are recommended.)
 - 7: To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber between the P-N1 terminals is recommended.
 - 8 : Two VNc terminals (9 & 16 pin) are connected inside DIP-IPM, please connect either one to the 15V power supply GND outside and leave another one open.
 - : It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
 - 10: If control GND is connected to power GND by broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point.
 - 11: The reference voltage Vref of comparator should be set up the same rating of short circuit trip level (Vsc(ref): min.0.43V to max.0.53V).
 - 12: OR logic output high level should exceed the maximum short circuit trip level (Vsc(ref): max.0.53V).



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